Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to further clarify Applicants invention.

No new matter has been added. Support for the amended claims are found in the previously presented claims, the Figures and/or the Specification

Claim Rejections under 35 USC 112

Claims 1-13 stand rejected under 35 U.S.C 112 first paragraph, as failing to comply with the written description requirement. Examiner asserts that the following underlined language is not supported in the Specification such that one of ordinary skill would understand that an inert gas plasma treatment does not include material deposition.

"then plasma treating the exposed gate dielectric and polysilicon layer in-situ with an inert gas plasma to neutralize an electrical charge imbalance, said plasma treatment performed

without material layer deposition."

Examiner quotes MPEP 2173.05(i) that "the mere absence of a positive recitation is no basis for exclusion. Any claim limitation containing a negative limitation which does not have basis in the original disclosure should be rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement".

Yet Examiner ignores further guidance:

> Any negative limitation or exclusionary proviso must have basis in the original disclosure. If alternative elements are positively recited in the specification, they may be explicitly excluded in the claims. See *In re Johnson*, 558 F.2d 1008, 1019, 194 USPQ 187, 196 (CCPA 1977) ("[the] specification, having described the whole, necessarily described the part remaining."). See also *Ex parte Grasselli*, 231 USPQ 393 (Bd. App. 1983), *aff 'd mem.*, 738 F.2d 453 (Fed. Cir. 1984). The mere absence of a positive recitation is not basis for an exclusion. Any claim containing a negative limitation which does not have basis in the original disclosure should be rejected under 35 U.S.C. 112, first paragraph as failing to comply with the written description requirement. **Note that a lack of literal basis in the specification for a negative limitation may not be sufficient to establish a *prima facie* case for lack of descriptive support.** *Ex parte Parks*, 30 USPQ2d 1234, 1236 (Bd. Pat. App. & Inter. 1993). See MPEP § 2163 - § 2163.07(b) for a discussion of the written description requirement of 35 U.S.C. 112, first paragraph.

Applicants respectfully refer Examiner to the following relevant portions of the MPEP and the case law:

> **ADEQUACY OF WRITTEN DESCRIPTION**
> ***A. Read and Analyze the Specification for Compliance with 35 U.S.C. 112, para. 1***
> Office personnel should adhere to the following procedures when reviewing patent applications for compliance with the written description requirement of 35 U.S.C. 112, para. 1. The examiner has the initial burden, after a thorough reading and evaluation of the content of the application, **of presenting evidence or reasons why a person skilled in the art would not recognize that the written description of the invention provides support for the claims.** There is a strong presumption that an adequate written description of the claimed invention is present in the specification as filed, *Wertheim*, 541 F.2d at 262, 191 USPQ; however, with respect to newly added or claims, applicant should show support in the disclosure for the new or amended claims.
>
> **"[I]n considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom."** *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968)
> It is now well accepted that a satisfactory description may be in the claims or any other portion of the originally filed specification.
> See MPEP, 8th Ed, Section 2163 (I)
> While there is **no *in haec verba* requirement**, newly added claim limitations must be supported in the specification through **express, implicit, or inherent disclosure.**
> See MPEP, 8th Ed, Section 2163 (I) (B)
> The fundamental factual inquiry is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed. See, e.g., *Vas-Cath, Inc.*, 935 F.2d at 1563-

> 64, 19 USPQ2d at 1117.
> Possession may be shown in many ways. For example, **possession may be shown by describing an actual reduction to practice of the claimed invention.** Possession may also be shown by a **clear depiction of the invention in detailed drawings** or in structural chemical formulas which permit a person skilled in the art to clearly recognize that applicant had possession of the claimed invention. **An adequate written description of the invention may be shown by any description of sufficient, relevant, identifying characteristics so long as a person skilled in the art would recognize that the inventor had possession of the claimed invention.** See, e.g., *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1323, 56 USPQ2d 1481, 1483 (Fed. Cir. 2000)

Examiner has not explained or provided a convincing line of reasoning outlining why one of ordinary skill would fail to understand that an inert gas plasma would result in not material deposition.

Applicants respectfully contend that one of ordinary skill would clearly understand that Applicants invention encompasses and **implicitly discloses, as would be understood by one of ordinary skill in the art that a plasma treatment of inert gas results in no material deposition or etching,** especially where the plasma treatment is disclosed as a treatment carried out following a second main etch and prior to an overetch step, and where the inert gas plasma treatment is carried out to neutralize a charge imbalance present from a previous etching step:

While Examiner is mistaken and has failed to make out a *prima facie* case that Applicants claim language fails to comply with the written description requirement, the claims have nevertheless been amended in an effort to further prosecution on the merits.

Claim Rejections under 35 USC 103

1. Claims 1-3, 5-8, and 14-15, and 16 stand rejected under 35 USC 103(a) as being unpatentable over Westerheim et al. (American Vacuum Society Sept./Oct 1998, pgs 2699-2706) in view of Wang et al.(6,127,278), Khan et al. (2003/0003748), and Hwang et al. (Applied Physics Letters 71(14), 6 October 1997, pgs 1941-1944).

Westerheim et al. disclose a method for etching a polysilicon gate electrode involving an **initiation etch** (Cl2/HBr) following removing **an organic ARC overlayer (to remove a native oxide** present on the polysilicon surface) (see C. 2., page 2701); **a single main etch** (Cl2/HBr) to endpoint detection of the gate oxide carried out with a moderate wafer bias (see C. e., page 2701) (also note the HBr is added to passivate the sidewalls of

the gate to prevent lateral etching of the gate)single main etch step); **and an overetch step where Cl2 is removed from the chamber and the HBr reduced and O2 added and where the overetch is carried out in two steps where the first step is "a short step at higher wafer bias to maintain directionality during the transition from the main etch" in order to reduce notching at the base of the polysilicon line.** The wafer bias is then reduced for the longer second overetch step (see C.4. page 2702).

Thus Westerheim et al. disclose a different process than Applicants to avoid notching of the polysilicon gate electrode, i.e., first removing Cl2 following the main etch step followed by a first overetch step with HBr/O2 and a "higher wafer bias to maintain directionality".

With respect to claims 1, Westerheim et al. fail to disclose the following elements of Applicants invention including those elements in **bold type**:

1. (currently amended) A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching including notching in a polysilicon gate electrode etching process comprising the steps of:

providing a semiconductor process wafer comprising a gate dielectric formed over a silicon substrate and a polysilicon layer formed over the gate dielectric;

providing a hardmask layer over the polysilicon layer;

carrying out a first reactive ion etch (RIE) step to etch through a thickness of the hardmask layer to expose the polysilicon layer to form a patterned hard mask for forming a gate electrode;

carrying out a second RIE step to etch through a first thickness portion of the polysilicon layer including an RF source power and an RF bias power;

carrying out a third RIE step to etch through a second thickness portion of the polysilicon layer to endpoint detection to expose portions of an underlying gate dielectric including using lower RF power compared to the second RIE step, said lower RF power selected from the group consisting of a lower RF source power and a lower RF bias power; and,

then plasma treating the exposed gate dielectric and polysilicon layer in-situ with an inert gas plasma consisting of

inert gas to neutralize an electrical charge imbalance."

Examiner is mistaken that Westerheim discloses providing a hardmask layer and then etching the hardmask layer to form a patterned hardmask layer. Westerheim disclose using an organic (soft) ARC layer which is cleared out from the bottom of a patterned photoresist layer (see C.1. pg 2701). A native oxide of less than 200 Angstroms of the polysilicon is removed from the bottom of the patterned photoresist layer following clearing out of the organic (soft) ARC layer (see C.2. page 2701).

In addition, Examiner erroneously equates the first overetch step of Westerheim with the inert gas plasma treatment of Applicants, despite the fact that Westerheim disclose that the first overetch step is an HBr/Cl2 etch chemistry carried out with a higher wafer bias and nowhere suggests or discloses an inert gas plasma treatment without an RF bias prior to an overetch step as Applicants have disclosed and claimed (see Applicants claims 2, 3 and 14).

See e.g., MPEP 2111.01:

> During examination, the claims must be interpreted as broadly as their terms reasonably allow. **This means that the words of the claim must be given their**

> **plain meaning unless applicant has provided a clear definition in the specification.** *In re Zletz,* 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).
>
> When not defined by applicant in the specification, the words of a claim must be given their plain meaning. **In other words, they must be read as they would be interpreted by those of ordinary skill in the art.** *In re Sneed,* 710 F.2d 1544, 218 USPQ 385 (Fed. Cir. 1983).

In contrast Wang et al. discloses a multi-step process for forming a **high aspect ratio trench** in silicon having a hardmask over the silicon using **HBr and O2 to form tapered openings** (80-89 deg; col 4, lines 47-55)) including forming a passivation layer that may be removed by HF prior to a **second etch step where SF6 is added to control the taper** of the trench to be more vertical (over 88 deg; col 4, lines 60-64) of the openings (see Abstract).

Wang et al. general teach that the first trench etch step is from 500 to 3000 Watts, the second trench etch step is at a lower source power from 500 to 1600 Watts and that the bias power can vary from 5 to 300 Watts (preferably at 400 kHz) (col 4, lines 5-9; lines 23-34). Wang et al. further teach that **increasing the bias power increases the taper angle** (col 5, lines 31-39) and therefore controlling the bias power in the first etch step is desirable whereas increasing the source power increases the etch

rate (col 5, lines 40-49).

There is no motivation to modify the polysilicon gate etch process of Westerheim with the silicon trench etch process of Wang et al. Examiner is further mistaken that Wang et al. teach that lowering the either the bias power or source power results in etched openings that are more perpendicular. Nevertheless, it is clear that Wang et al. nowhere suggest that the silicon trench etch process including the addition of SF6 or controlling a bias power to control the taper angle of a trench could be successfully used in a polysilicon gate etch process. Moreover, modification of Westerheim to have the polysilicon etch process carried out at lower bias power to reduce a taper angle would change the principle of operation of the gate etch method of Westerheim and make it unsuitable for its intended purpose.

Even assuming arguendo, a proper motivation for modifying Westerheim based on the teachings of Wang et al., such modification does not help Examiner in producing Applicants invention, including Applicants inert gas plasma treatment.

"**First**, there must be some **suggestion or motivation**, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the

reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success. Finally**, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"Finally, when evaluating the scope of a claim, every limitation in the claim must be considered. Office personnel may not dissect a claimed invention into discrete elements and then evaluate the elements in isolation. Instead, the claim as a whole must be considered." See, e.g., *Diamond v. Diehr*, 450 U.S. at 188-189, 209 USPQ at 9.

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).*

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art

invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

With respect to claims 2, 3, and 14, the fact that Khan et al. further teach a **pulsed bias power** (paragraph 0021) **in etching trenches in silicon over an SiO2 insulator** with an **SF6/O2 etching chemistry** (see paragraphs 001; 0020) to **avoid notching** at the silicon-insulator interface **at the bottom of the trench** including first depositing a polymer passivation layer over patterned photoresist prior to etching the trenches (paragraphs 0018, 00019) and a **second polymer deposition step without bias power is made (see claim 8) prior to overetching the bottom of the trench** at the silicon/insulator interface (paragraph 0022) and **using the same pulsed bias power in the overetch step as in the main trench etch step**(paragraph 0022), does not further help Examiner in producing Applicants invention.

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Examiner is mistaken in asserting that Khan et al. disclose an overetch step without a bias power.

In addition, even assuming arguendo a proper motivation for modifying the completely different gate etch process of Westerheim with the silicon trench etch process of Khan et al., such modification would **change the principle of operation** of the overetch process of Westerheim who discloses a first overetch step with higher DC bias (produced by RF power) (not pulsed power) to maintain directionality of the etch and a second longer overetch with moderate bias, **making it unsuitable for its intended purpose.**

Nevertheless, such modification does not produce Applicants invention including Applicants inert gas plasma treatment following exposure of portions of an underlying gate dielectric.

"**First,** there must be some **suggestion or motivation,** either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second,** there must be a **reasonable expectation of success. Finally,** the prior art reference (or references when combined) **must teach or suggest all the claim limitations.** The teaching or suggestion to make the

claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).*

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

"we do not pick and choose among the individual elements of

assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination". Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).

With respect to claims 6 and 16, the further fact that Hwang et al. teach adding an inert gas (e.g., He) to a Cl2/BCl3 plasma (see first paragraph, page 1942) in an overetch step in a polysilicon gate etch process, does not further help Examiner in producing Applicants invention.

"we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination". Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).

2. Claims 4, 9, 11-12, 17-19, and 21-22 stand rejected under 35 USC 103(a) as being unpatentable over Westerheim et al. in view of Wang et al, Khan et al., and Hwang et al., above, and further in view of Lee (5,665,203).

Applicants reiterate the comments made above with respect to Westerheim et al. in view of Wang et al, Khan et al., and Hwang et al.

Even assuming *arguendo* a proper motivation for further modifying Westerheim et al. based on the teachings of Lee et al., the fact that Lee et al. teaches that the polysilicon layer includes both n and p doped regions to form doped polysilicon gate electrodes shown in parallel in with a hardmask (and without a resist mask (col 4, lines 31-35) using a completely different etch chemistry than Westerheim i.e., a first polysilicon etch is carried out using **HBR/CL2/O2** (col4, lines 34-36) and then **HBR/O2** in a **second polysilicon etching step** col 4, lines 52-67)**which includes the overetch process** (col 2, lines 1-5; col 4, lines 52-64), and where the Cl2 is removed from the etching chamber between the first polysilicon etch step and second polysilicon etch step, such modification of Westerheim does not further help Examiner in producing Applicants invention.

It is noted that Lee et al. nowhere recognize the problem of forming notches during the gate electrode etching process, but rather only recognizes that an n-doped gate structure etches faster **anisotropically** (vertically) than a P gate structure using HBr/Cl2 plasma etching chemistries (see col 1, lines 20-29; col

5, lines 30-45).

"**First**, there must be some **suggestion or motivation**, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success**. **Finally**, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984)*.

3. Claims 10, 13, 20, and 23 stand rejected under 35 USC 103(a) as being unpatentable over Westerheim et al. in view of Wang et al, Khan et al., and Hwang et al., above, and further in view of Lill et al. (US 6, 284,665).

Applicants reiterate the comments made above with respect to Westerheim et al. in view of Wang et al, Khan et al., and Hwang et al.

Even assuming arguendo a proper motivation for using the teachings of the completely different **polysilicon etchback (planarization etching) process with an underlying silicon nitride layer** of Lill to modify the polysilicon gate etch process of Westerheim et al., the fact that Lill discloses the use of a **low bias voltage** in the range of 50 to 100 Volts (including no bias power) to avoid ion damage to the gate oxide layer (col 2, lines 46-49) **during polysilicon etchback (planarization etching) process with an underlying silicon nitride layer**, does not further help Examiner in producing Applicants invention.

"**First**, there must be some **suggestion or motivation**, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success**. **Finally**, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success

must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination". Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).

4. Claims 10, 13, 20, and 23 stand rejected under 35 USC 103(a) as being unpatentable over Westerheim et al. in view of Wang et al, Khan et al., and Hwang et al., above, and further in view of Wolf et al. (Silicon Processing for the VLSI Era; Vol 1; 1986; Lattice Press).

Applicants reiterate the comments made above with respect to Westerheim et al. in view of Wang et al, Khan et al., and Hwang et al.

Even assuming arguendo, a proper motivation for modifying the method of Westerheim et al. based on the teachings of Wolf,

the fact that Wolf teaches that producing reproducible etch processes are a challenge due to the large number of parameters including macroscopic parameters such as feed gas power and pressure and where the effect of changing any single parameter is not well understood and that a change in any single macroscopic plasma process parameter can alters two or more basic plasma parameters and one or more surface plasma parameters including temperature and **electrical potential** makes process development in plasma system a challenge (see page 547), does not help Examiner in producing Applicants invention, but rather underscores the fact that Applicants invention is unobvious and that Examiners attempted modification of Westerheim et al. disparate references dealing with unrelated etching processes in an effort to reproduce Applicants invention provides no motivation for modification or expectation of success.

Further, Examiners attempted use of the general teachings of Wolf. (who discloses that factorial design experiments may be used to obtain information from unknown or poorly understood phenomena to help develop and optimize processes), to modify Westerheim et al, amounts to a "routine experimentation" argument.

However, Examiner has not shown Applicants process in the

prior art or that Applicants parameters have a recognized result.

"A particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation." *In re Antonie*, 559 F.2d 618, 195 USPQ 6 (CCPA 1977).

Moreover, none of the cited references, singly or in combination, provide Applicants method and solution to the problem that Applicants have solved by their disclosed and claimed invention,

"A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching **including notching** in a polysilicon gate electrode etching process".

Moreover, none of the cited references suggest or disclose Applicants polysilicon gate electrode etch process in combination with Applicants inert gas plasma treatment "to neutralize an electrical charge imbalance".

"**First**, there must be some **suggestion or motivation**, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success**. **Finally**, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

Conclusion

The multiple (six) cited references, alone or in combination, fail to produce or suggest Applicants disclosed and claimed invention and therefore fail to make out a *prima facie* case of obviousness with respect to Applicants independent and dependent claims.

Applicants have amended the claims to further clarify their claim language and respectfully request favorable consideration by Examiner.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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